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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,895	04/20/2004	Sankaranarayanan Srinivasan	X-1544 US	5847

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

BV

Office Action Summary	Application No.	Applicant(s)	
	10/828,895	SRINIVASAN, SANKARANARAYANAN	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/828,895 filed 04/24/2004.

2. Claims 1-21 are pending in the Application.

Specification

3. The abstract of the disclosure is objected to because it is not clear what Applicant intend to mean by phrase "A final delay for connections of the circuit design can be predicted were connection overlaps to be removed". For examination purposes Examiner replaces "were" by If or when.

Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1, 8, 15 are objected to because of the following informalities: within similar to the Abstract problem with further assuming "were" on the line 9 of the claims 1 and 8 and line 10 of the claim 15 as if or when.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: there is missing step/relationship between second and third limitations of the claims 1, 8 and 15, such as: under what condition and when "connection sharing has been removed" and how steps (second and third limitations) are related to a statement of the preamble of the independent claims 1, 8 and 15 "relieving timing-based congestion".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 5-8, 12-15 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Ramachandran et al. (US Patent Application Publication 20040243953).

With respect to claim 1 Ramachandran et al. teaches a method of detecting and relieving timing-based congestion during physical implementation of an integrated circuit within a method for automatically modification a circuit design including determination of violated constraints, such as timing parameters, congestion etc. (abstract, paragraph [0033]), said method comprising: routing connections of a circuit design for the integrated circuit in a delay mode within logic synthesis tool for creating a

logic element network (routing in the circuit design) during a global routing (paragraph [0042]), wherein the logic synthesis tool is capable to restructure the logic based on a optimization of delay (delay mode) (paragraph 0028]) as shown on the Fig. 3 by step 221 (paragraph 0070]); calculating an initial delay for the connections of the circuit design within timing engine embedded into synthesis tool for estimating sensitivity in the timing parameters (initial delay) (paragraph 0032]); predicting a final delay for the connections of the circuit design were connection sharing has been removed within global route estimation to predict congestion map of the route (paragraph [0042]) and removing this congestion by reducing sensitivity in the instance in the congested area to prevent timing violations after detailed routing (paragraph [0044]), wherein removing the congestion is done, for example, by increasing the length of wire (paragraph [0046]), which will affect timing objective parameter calculated based on the predicting and removing congestion during the global routing (paragraph [0051]); identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial and final delays within the synthesis tool performs transformations in predicted congestion routing to ensure that the changes in the timing objective is insignificant in relation to the timing constraints (paragraph [0032]); and selectively performing a detailed routing of the circuit design or further optimizing the identified connections of the circuit design according to said identifying step within the synthesis tool performing modification of the circuit design on the selected portion of the circuit having higher probability in violating timing constraints in the iterative mode as detailed routing (paragraph [0031]).

With respect to claims 8 and 15 Ramachandran et al. teaches routing connections of a circuit design for the integrated circuit in a delay mode within logic synthesis tool for creating a logic element network (routing in the circuit design) during a global routing (paragraph [0042]), wherein the logic synthesis tool is capable to restructure the logic based on a optimization of delay (delay mode) (paragraph 0028]) as shown on the Fig. 3 by step 221 (paragraph 0070]); calculating an initial delay for the connections of the circuit design within timing engine embedded into synthesis tool for estimating sensitivity in the timing parameters (initial delay) (paragraph 0032]); predicting a final delay for the connections of the circuit design were connection sharing has been removed within global route estimation to predict congestion map of the route (paragraph [0042]) and removing this congestion by reducing sensitivity in the instance in the congested area to prevent timing violations after detailed routing (paragraph [0044]), wherein removing the congestion is done, for example, by increasing the length of wire (paragraph [0046]), which will affect timing objective parameter calculated based on the predicting and removing congestion during the global routing (paragraph [0051]); identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial and final delays within the synthesis tool performs transformations in predicted congestion routing to ensure that the changes in the timing objective is insignificant in relation to the timing constraints (paragraph [0032]); and selectively performing a detailed routing of the circuit design or further optimizing the identified connections of the circuit design according to said identifying step within the synthesis tool performing modification of the circuit design on the selected portion of the

circuit having higher probability in violating timing constraints in the iterative mode as detailed routing (paragraph [0031]). Wherein all steps of the method for automatically modifying a circuit design using synthesis solutions described in the claim 1 above are implemented within an apparatus (paragraph [0010]) by using computer system depicted on the Fig. 1 including computer readable media (paragraph [0012]).

With respect to claims 5-7, 12-14, 19-21 Ramachandran et al. teaches:

Claim 5: the predicting step further comprising using a quadratic model to predict the final delay within predicting (computing) timing objective parameters as complex function of multiple parameters, such as length of the path, capacitance and other parameters using any curve fitting techniques (paragraphs [0051], [0049]);

Claim 6: the step of further optimizing the circuit design comprising at least one incrementally placing the circuit design or performing physical synthesis on the circuit design within logic synthesis tool producing the design of IC and making changes in routing components (cells) when timing requirement s are not met (paragraph [0028]);

Claim 7: the step of further optimizing the circuit design comprising rerouting connections changed by the incrementally placing step within logic synthesis tool producing the design of IC and making changes in routing components (cells) when timing requirement s are not met (paragraph [0028]), wherein a predicted congestion map of the routes is determined (paragraph [0042]) with further changes according to the predicted and removed congestion in the layout (paragraph [0045]).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-4, 9-11, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramachandran et al. as applied to claims 1, 8 and 15 above, and further in view of Harn (US Patent Publication 20040040007).

With respect to claims 2-4, 9-11, 16-18 Ramachandran et al. teaches the limitations from which the claims depend. However even Ramachandran et al. discloses calculating of the delay during global routing with predicting congestions in the routing and removing this congestion with further prediction (calculation) of the delay in the routing and selectively performing rerouting (detailed touting), but lacks the specifics regarding predicting final delay for the connections. Harn teaches:

Claim 2: for each connection, said predicting step comprising: determining a number of connections sharing each wire by said routing step; summing the number of connections for each wire; and adding the initial delay to a product of the summed number of connections and the initial delay within generating trial routing plan by placement and routing tool (P&R) including calculating a routing congestion factor (paragraph [0071])), wherein P&R tool computes routing demand factor for each block as a sum of the areas, i.e. all nets within the block and wherein two nets overlap the sum is added twice (paragraph [0071]);

Claim 3: the summing step comprising multiplying the summed of connections by a weighting factor as shown in the example of calculating cost function P&R tool multiplies overflow factor (containing all routing nets/connections) by weighting factor (paragraph [0075]);

Claim 4: the step of adding the initial delay comprising first multiplying the product by weighting factor within adjusting the weighting factor by adding delay of problematic path (paragraph 0075]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Harn to teach the specifics subject matter Ramachandran et al. does not teach, because routing congestion is eliminated by estimating routing congestion in various areas of the layout and relocating each cell to least routing congested area (abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

Paul Dinh

PAUL DINH
PRIMARY EXAMINER